

BACKSIDE POWER DELIVERY · WAFER BONDING

Resolving AlN Bonding Films for Backside Power Delivery with FASTR

Laser Thermal measured a 1 μm PVD AlN film on TEOS oxide and on silicon with FASTR, fitting its FDTR and SSTR data jointly. The film conducts 92 W/m·K cross-plane and 41 W/m·K in-plane, the AlN/Si interface adds 5.7 $\text{m}^2\text{K/GW}$, and SSTR confirms the FDTR solution within 2%. A micron of this film plus its interface resists heat about sixty times less than a micron of the TEOS in the same stack.

Why AlN at the bonding interface

Backside power delivery (BSPDN) bonds the device wafer to a carrier and thins it to submicrometre silicon, which puts the bonding dielectric, usually silicon oxide, in the main heat path. TSMC researchers estimate BSPDN can raise device self-heating by about 30% compared with front-side delivery [1].

IBM's BSPDN simulations found AlN bond layers less sensitive to thickness than oxide [2], and PVD AlN is now being evaluated for permanent wafer bonding [3]. AlN is an insulator with a 6.1 eV bandgap and about 300 W/m·K bulk conductivity, but thin films are anisotropic and often interface-limited [1].

Why FASTR

FASTR runs FDTR and SSTR on one instrument. FDTR partitions a stack into films and interfaces but needs a heat capacity. SSTR measures total resistance without one, so a parameter set that must satisfy both cannot hide a correlation either mode alone would allow.

	FDTR	SSTR
Heat capacity	Required	Not used
Resolves	Individual films and interfaces	Total resistance under the spot
In-plane k	Weak with co-located beams	Sensed through $\sqrt{(k_z \cdot k_r)}$
Role in the fit	Partitions the stack	Bounds the total resistance

Samples

Two blanket wafers each carry a 1 μm AlN film deposited via PVD under an 80 nm Al transducer. On Sample B the silicon pulls heat straight down, which makes the film hard to see on its own. On Sample A, 4 μm of TEOS oxide blocks the vertical path, so heat must spread laterally through the AlN. The oxide also mimics the amorphous dielectric AlN grows on over a capped device wafer.

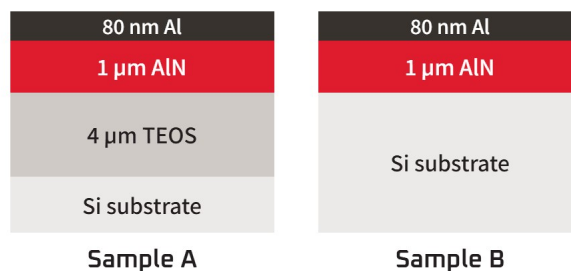


Figure 1. Sample stacks, not to scale. All results are from the wafer centers.

Measurement

Each stack was measured on FASTR at the wafer center with a 10 $\times$ objective, using two FDTR sweeps from 1 kHz to 33.5 MHz and five SSTR power sweeps through the same transducer. Both stacks were fitted together with one shared AlN film and their own Al/AlN interfaces, with SSTR entering as a 2% constraint on the 1 kHz amplitude.

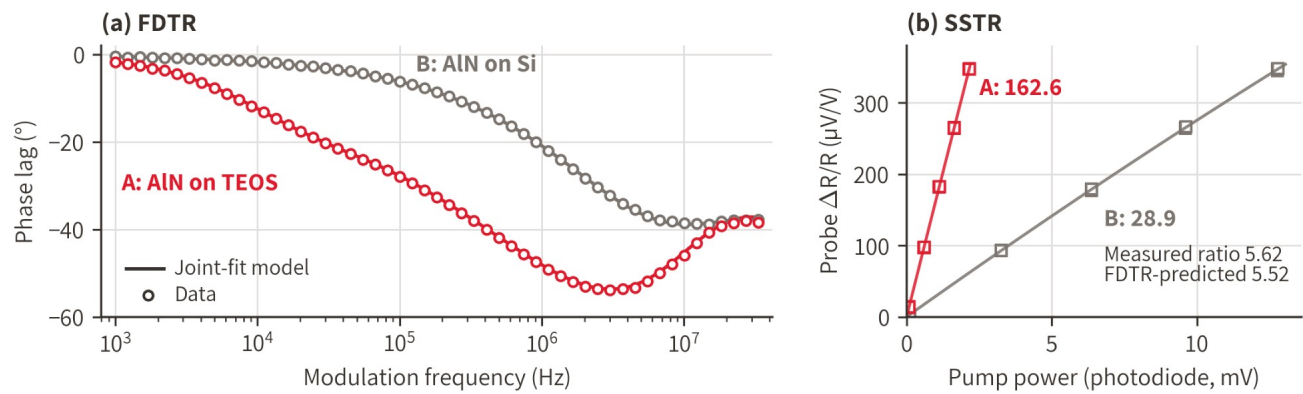


Figure 2. (a) FDTR phase spectra at the wafer center with the joint-fit model. (b) Five SSTR pump-power sweeps per stack with fits. Labels give the fitted slopes, and their ratio is compared with the FDTR solution's prediction at 1 kHz.

Table 1. FASTR joint-fit results, one shared AlN film across both stacks.

AlN film	Value	Interfaces and underlayer	Value
Cross-plane k (W/m·K)	92 ± 5	AlN/Si interface (m ² K/GW)	5.7 ± 1.1
In-plane k (W/m·K)	41.4 ± 3.7	Al/AlN, on Si / on TEOS (m ² K/GW)	2.67 / 2.46 ± 0.25
Total, Al to Si, Sample B (m ² K/GW)	19.3 ± 1.4	TEOS k, 4 μm (W/m·K)	1.02 ± 0.09

Uncertainties combine fit error with systematics in spot size, γ, the Al transducer, heat capacities, thicknesses, k_{Si} and FDTR bandwidth.

Results

Each stack answers a different question. On TEOS, heat has to spread sideways through the AlN, so FASTR measures the film's in-plane conductivity alongside its cross-plane value. On silicon, with the film already characterized, the measurement isolates the AlN/Si interface.

As an independent check, the FDTR results predict that the TEOS stack heats 5.52 times more than the silicon stack at the same power. SSTR measures 5.62, agreement within 2% with no calibration constant involved.

How SSTR bounds the fit

SSTR fixes the total thermal resistance under the spot without a heat capacity, so any parameter set FDTR returns has to reproduce it. On Sample A, where heat spreads laterally over the oxide, it adds a second, independent handle on in-plane conductivity.

What it means for integration

The film is anisotropic by a factor of 2.2, tracking the roughly 100 and 40 W/m·K reported for 200 °C sputtered AlN [1]. The AlN/Si interface, about 175 MW/m²K, is at or above the 150 MW/m²K typical of AlN on silicon and oxide [1]. It is a third of the film-plus-interface resistance, a share that grows as bond layers thin.

Why the whole system matters. Measured with FDTR alone, the silicon stack returns an in-plane value of 27 W/m·K, a third below the joint answer, because heat on silicon barely spreads sideways. FASTR removes that freedom with a second mode and a second stack, resolving both AlN conductivities, both interfaces and the TEOS underlayer, with SSTR closing on the FDTR solution within 2%.

References

[1] W.-Y. Woon et al., Thermal management materials for 3D-stacked integrated circuits, Nat. Rev. Electr. Eng. 2, 598–613 (2025).
[2] E. Y. Wu, T. Ando et al., Predictive simulations and experimental study of AlN bonding for better thermal dissipation in BSPDN, IBM Research.
[3] A. Tuchman et al., Development of high thermal conductance wafer bonding interface with PVD aluminum nitride, IEEE ECTC (2025).